Precision Phase Noise Measurements Using The Agilent 89410A Vector Signal Analyzer

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Introduction

The characterization of phase noise (timing jitter) of clocking sources has become crucial due to their direct impact on the performance of the data conversion devices (A/D and D/A). In particular modern Digital Low Level RF Systems have stringent requirements for RF amplitude and phase stability, and require extremely low phase noise clock sources. As an example: the CEBAF 1497 MHz RF system, after down conversion, 70 MHz (F70), will be sampled with a 56 MHz clock (Digital Down Conversion). To maintain amplitude (0.01%) and phase (0.1°) accuracy a maximum 1ps rms. time jitter is permitted. On the other hand: using an N bit ADC sampling at **f** frequency, the analog signal clock jitter should be smaller than $1/(\pi * \mathbf{f} * 2^{(N+1)})$ to keep system signal to noise (SNR) ratio small . For F_{70} and a 12 bit ADC the result is 0.55 ps . The average time jitter of a free running VCXO (voltage control crystal oscillator) is 10-100 ps , wrapping a PLL system around it can reduce it down to ~1 ps . To facilitate these measurements a LabVIEW program was developed using an Agilent Vector Signal Analyzer (VSA 89410A DC-10MHz). This note discusses these measurements.

Phase Noise and Jitter

Phase noise (frequency domain) or related time jitter (time domain) describes performance of our clock reference. In addition we will use the common term: single-sided phase noise density $S_{\Delta\theta}(f)$ expressed in radian^2/Hz which describes RMS phase distributions per measured bandwidth BW.

$$S_{\Delta\theta}(f) = (\Delta\theta)^2/BW \qquad [1]$$

Where $\Delta\theta$ is phase modulation (RMS). Usually SSB phase noise is given logarithmically:

$$S_{\Delta\theta}(f[dBc/Hz] = 10\log_{10}(S_{\Delta\theta}(f)) \qquad [2]$$

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Signal sources:

For our measurement we need a 10 MHz locked, phase coherent signal generator. 10 MHz reference from the VSA will be used for our VCXO PLL system and locked to the signal generator. RF output will be used to down convert the signal-under-test (F_{56}) into the 0-10 MHz VSA input bandwidth. All devices used will contribute to final phase noise. To ensure that test result reflect the performance of device-under-test rather than

signal sources or VSA, an ultra low noise signal generator is used simultaneously with VSA noise subtraction.

Setup:

Figure 1 illustrates setup used for phase noise measurement. RF amplifier is optional, input signal should be as big as possible without causing ADC overload.

Special care is required for the down conversion process. In Fig.1 a simple mixing operation is shown, however there are a number of pitfalls, particularly for high frequencies. Image protection or filtering may be necessary. Depending on down conversion method (type of mixer), spurious signals may be generated, causing additional noise.

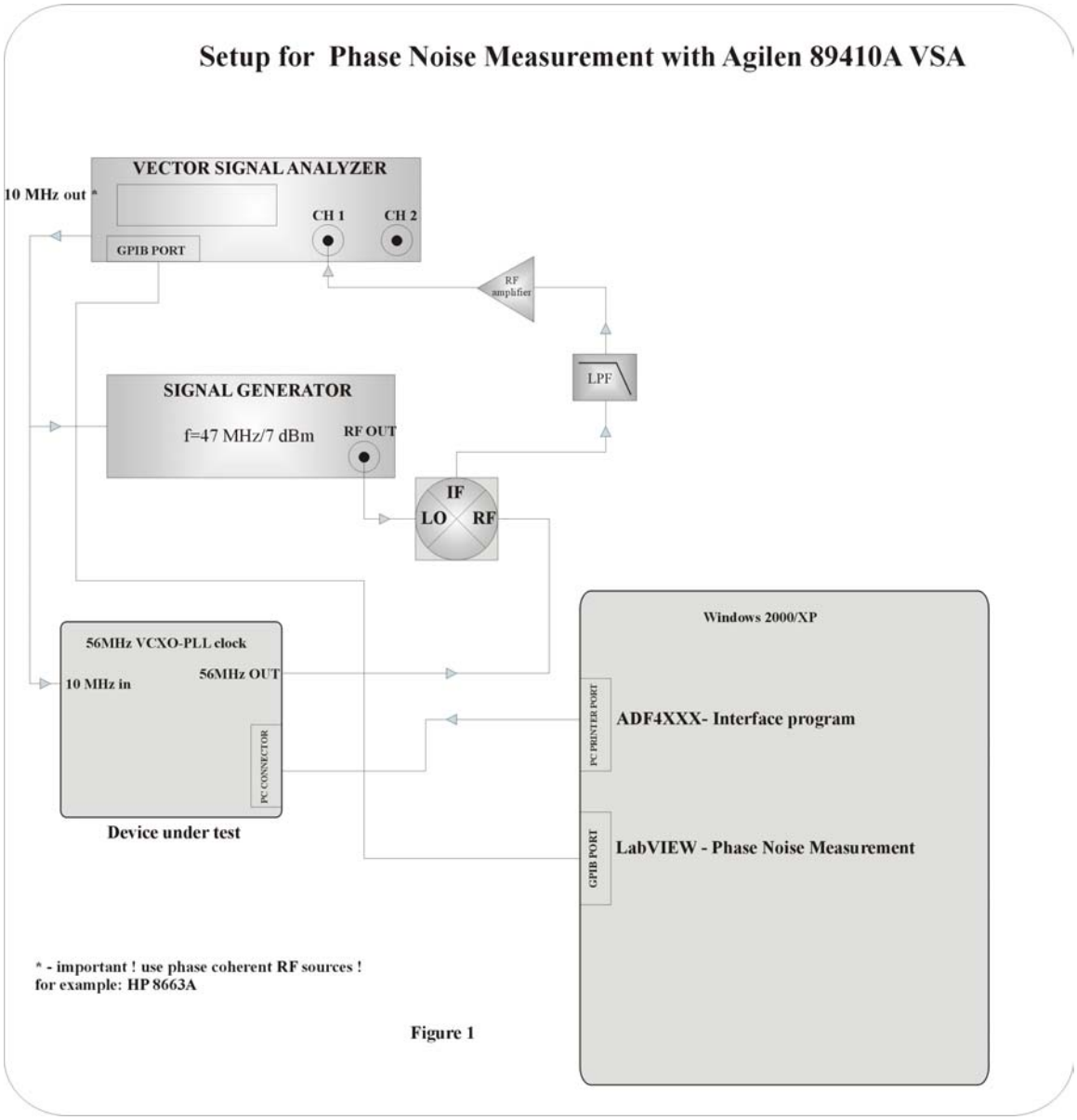


Figure 1

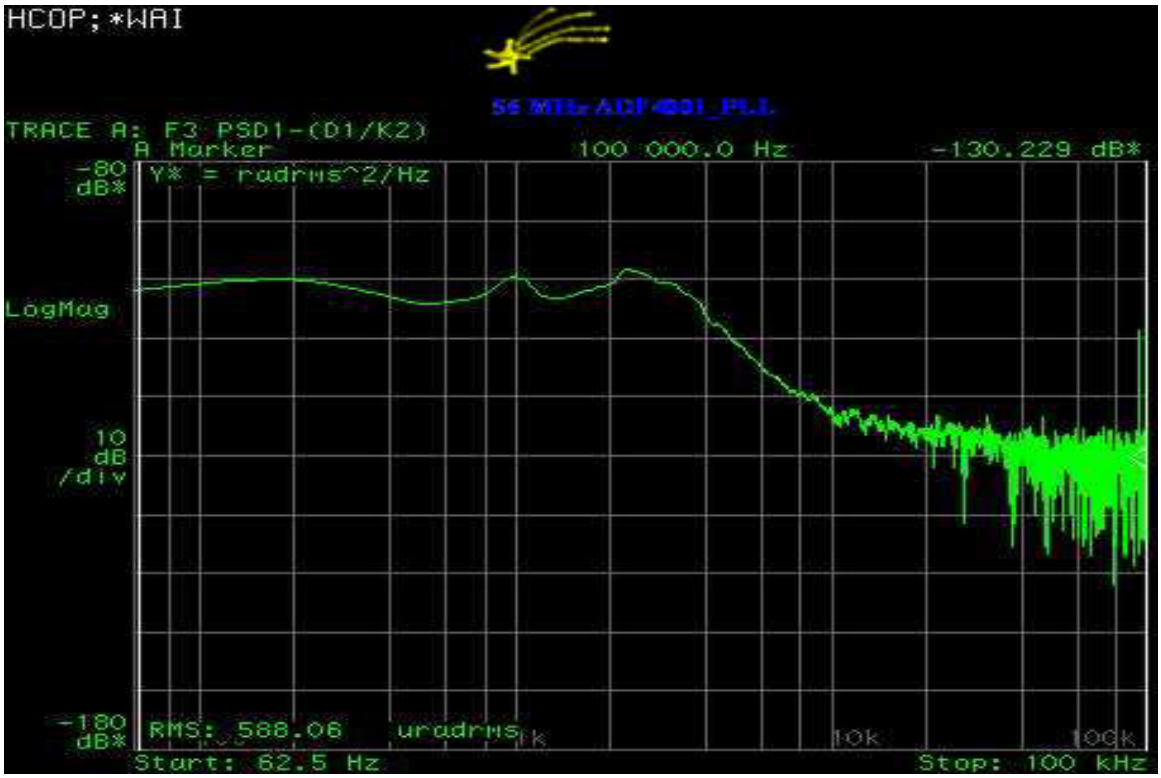
We tested 56 MHz VCXO-PLL clock based on ADF4001 clock generator controlled by ADF4XXX software from Analog Devices. SSB phase noise of 56MHz VCXO , typically values are 10 Hz –65dBc/Hz , 1kHz -115dBc/Hz , 10kHz -130dBc/Hz .

Measurement:

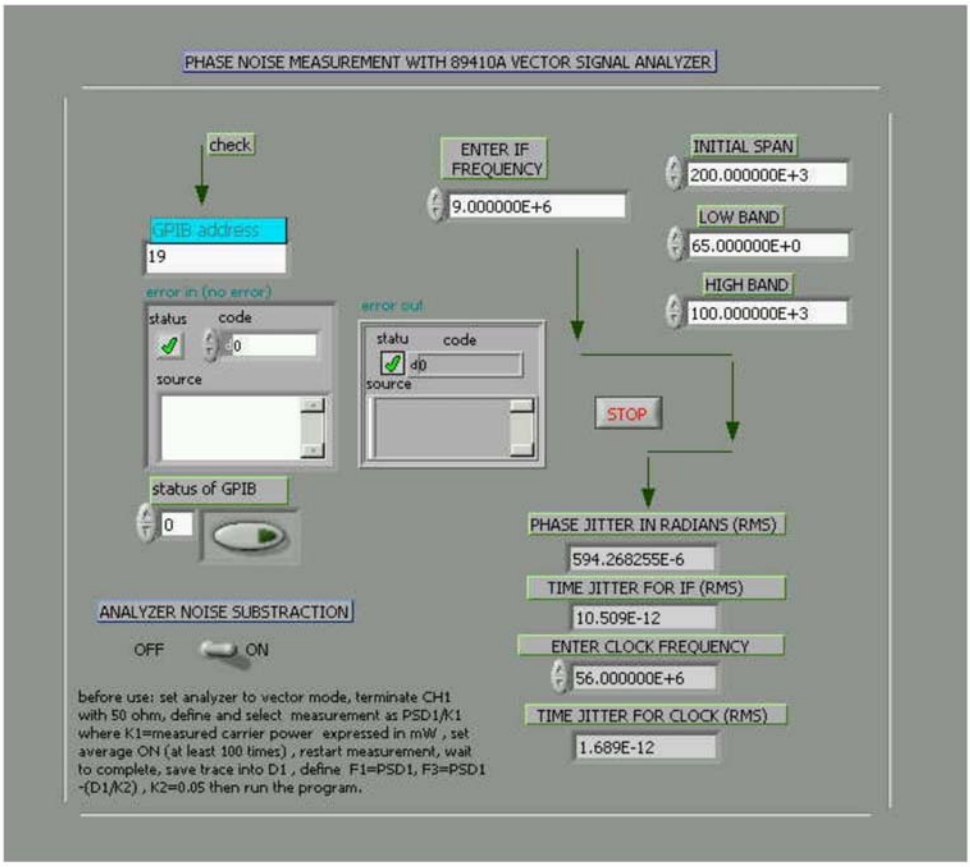
For VSA, mentioned above the SSB phase noise density $S_{\Delta\theta}(f)$ measurement is facilitated by the VSA math function and a LabVIEW program.

The defined function F1=PSD/K1, where K1=$10^{\text{carrier power[dBm]}/10}$ and PSD is the measured power spectral density, and corresponds to $S_{\Delta\theta}(f)$ as long as entire noise is dominated by phase noise rather than AM modulation. For heavily modulated carrier the same

formula can be used, however the carrier power has to be measured using band-power markers. Such a process is known as a adjacent-channel power measurement.
After direct SSB phase noise density measurement is completed, LabVIEW will continue to perform the Phase Perturbation measurement that includes phase jitter, time jitter, and RMS phase deviation. This process uses a built-in function, PM Demodulation, together with band-power markers (RMS measurement) and averaging to reduce variance of single PSD trace. Illustration bellow shows VSA screen during this process.



The Measurement can be improved by removing the effect of the VSA's own input noise. This process is facilitated with LabVIEW too, but an additional measurement must be performed prior to the final test. This test includes terminating the CH1 VSA input into 50 ohms and saving the averaged carrier power corrected measurements (several hundred) executed in Vector Mode (no PM mode). The measurement illustrated on the picture above is already included this correction. The illustration on next page presents a LabVIEW screen during phase perturbation identification.



Conclusion:

The phase noise measurement with VSA due to its ability to perform fast, direct phase noise measurement in any domain is easy and comfortable. The capability to mathematically lock to drifting carriers allowing accurate averaged measurement is not available for regular spectrum analyzers. The phase noise measurement with VSA is limited by the analyzers own input noise. Using PM demodulation Auto carrier function makes any oscillation varying around 0° invisible, and as a result of the locking action of this function; the two lowest demodulated frequency points are invalid.

References:

1. *Measuring Phase Noise with the Agilent 89400 Series VSA* . Agilent PN 894400-2
2. *Downconverted Measurements Using HP 89410A and HP 89411A.* HP Product Note 89400-9
3. *Phase Noise Performance of the HP 89400 Series.* HP Product Note 89400-11
4. *PSG/ESG Phase Coherency between multiple PSG's/ESG's* Agilent Technologies / Signal Source Division
5. *Trends in high speed, low power Analog to Digital converters.* L. Dugoujon , STMicroelectronics