Performance and Technical Requirements for the CEBAF Energy Upgrade Low Level RF System

Hai Dong
Alicia Hofler
Curt Hovater
John Musson

Thomas Jefferson National Accelerator Facility
12000 Jefferson Avenue
Newport News, Virginia 23606

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INTRODUCTION

The 12 GeV CEBAF Energy Upgrade will increase the beam energy from 6 GeV to 12 GeV. To support this 80 new SRF acceleration systems are to be added to the accelerator, 40 in each linac, divided up into 10 new 100 MeV cryomodules. The upgrade cryomodules will incorporate new features like Piezo tuners and operate at much higher gradients such that using the present Low Level RF (LLRF) controls is impractical with out reducing the performance of the upgrade cryomodules. Many of the analog components of the present LLRF system are now obsolete or hard to find. In addition with the advances in the hardware for digital signal processing, a digital controller is more attractive. Therefore we have decided to procure new LLRF controls based on digital technology.

The energy upgrade project is currently at the CD0 milestone and we expect to reach CD1 shortly. With that in mind we expect to be completing the LLRF R&D phase within 2006 and moving on to the pre-engineering development in 2007. The final LLRF design should be ready by the middle of 2008 for production.

The purpose of this document is to have a set of requirements that can be used to guide hardware/software designs and settle issues concerning the new LLRF system. To further guide the LLRF design, the requirements document has been extended to include both a functional design criteria and hardware specifications. As applicable as possible the requirements are mostly hardware non-specific. The chapters of this document have been divided up into the following:

1. Chapter One: Top level and performance requirements concerning accelerator physics issues, operability and maintenance.

2. Chapter Two: LLRF functional requirements, which will guide both the embedded firmware and the high level software design.

3. Chapter Three: Transceiver requirements which will guide the RF and analog hardware design.

4. Chapter Four: Digital requirements which will guide the FPGA and embedded processor design.

5. Chapter Five: Cavity Resonance Control, Heaters and Interlocks requirements specific to CEBAF cryomodules.

Performance and Technical Requirements for the CEBAF Energy Upgrade LLRF System

1.0 INTRODUCTION

This chapter contains the top level performance requirements needed to design the LLRF system for the CEBAF energy upgrade. These requirements are derived from accelerator physics, operational and maintenance requirements.

1.1 Requirements for Amplitude and Phase Field control are shown below in table 1.1 The rms. field regulation must be continually monitored for system performance (as is the case now). Cavities with poor regulation must be signaled through EPICS and the RF alarm handler.

Table 1.1 Cavity Field Regulation Requirements*

	Fast (< 1 sec)	*Slow (> 1 sec)*
Phase Stability (correlated) rms.	0.24^{o}	infinite
Phase Stability (un-correlated) rms.	0.5^{o}	3.0^{o}
Amplitude (correlated) rms.	2.2×10^{-5}	NA
Amplitude (un-correlated) rms.	4.5×10^{-4}	NA

* For gradients between 2 and 25 MV/m

1.2 Scalar set points for amplitude and phase during operation. Set point resolution will be 0.1% and 0.1 degree for amplitude and phase respectively.

1.3 Feed forward capability including adaptive feed forward (for injector and pulsed operations). The implementation shall provide for operation with or without feed forward. When feed forward is enabled, the system shall provide for either static or adaptive operation. The feed forward implementation shall rely on tables that can be accessed via EPICS.

1.4 Filtering of the RF drive and/or cavity field probe signals to prevent excitation of nearby cavity modes and to reject nearby modes that are excited by the beam. This can be done either in the analog section or with in the digital section.

1.5 The control loop PID parameters/gain (K_P, K_I, K_D) shall be adjustable from an EPICS screen. In addition the gains will also be adjustable as phase and amplitude gain parameters.

1.6 Loop gain will be independent of the gradient set point.

1.7 Latency: Overall system latency should be compatible with obtaining the field control required given the technology chosen. An ideal latency budget should be similar to table 1.7.

Table 1.7 RF System Latency Budget

Subsystem	Latency
Cables, Klystron, waveguide	150 ns
Transceiver	100 ns
Digital section	500 ns
Total	750 ns

1.8 Variable frequency mode for resonance hunting. This mode of operation shall be used whenever a cavity is brought into operation from an idle state. Resonance hunting provides for determining the cavity resonant frequency. The cavity tuning error shall be reported as a process variable, and LLRF processor shall operate the stepper motor to tune the cavity frequency to nominal 1497 MHz. There are multiple ways of accomplishing this including using self excited loop or a direct digital synthesis routine within the firmware. The amplitude regulation requirement shall be relaxed to ±5% and there shall be no phase regulation requirement when in variable frequency mode.

1.9 Resonance control. The RF control system shall calculate the difference between the reference frequency and the cavity resonant frequency during normal linac operation without impacting beam delivery. The frequency detuning (in Hz) shall be available as a process variable updated at a minimum rate of 0.2 Hz. The correction will be handled by EPICS for the stepper motor control and internally to the LLRF using the PZT. Tuning accuracy is ~ 2 Hz (cryomodule specification).

1.10 History buffers that provide for an EPICS display of the following wave forms:

a. Incident (forward) RF Power
b. Reflected RF Power
c. Cavity Field
d. Drive Signals (I & Q or phase & amplitude)
e. Internal Diagnostic Signals, e.g., loop error, as necessary for system setup

The waveforms shall be obtained in either CW or pulsed mode (typically 60 Hz as determined by the electron source). The EPICS display of these waveforms shall be updated on the occurrence of an event with a maximum update rate of 6 Hz. All signals shall be displayable in either amplitude/phase or real/imaginary format. At least 20 ms of waveform shall be displayed so that the cavity fill, beam-on/off, and cavity field decay can be observed. The display resolution shall be 2 us (10,000 points). At least three of the five waveforms shall be displayable simultaneously.

1.11 Cavity arc and quench detection. The RF drive and the interface to the CEBAF Fast Shut Down system (FSD) shall be inhibited within 10 μs of the detection and shall remain inhibited until beam is off. They shall be re-enabled once beam has been off for 100 ms and/or when the arc is extinguished and/or when the vacuum is normal.

1.12 Consecutive faults shall result in latching the RF drive and FSD inhibits to prevent automatic resumption of operation without operator intervention. The maximum number of permitted consecutive faults shall be settable by system experts (see chapter 2 and 5).

1.13 Modes of operation. The LLRF control system must accommodate operation for both pulsed and cw beam operations. In addition the system needs to be able to operate both in open and closed loop modes.

1.14 External Inputs: The LLRF system shall have a beam sync and accommodate both a fast feedback and feed forward system (analog inputs must have at least 10 kHz bandwidth). See chapters 2 – 5.

1.15 External Outputs (non EPICS): High Power Amplifier interface (RF drive, various interlock/permits, described in detail in the chapters 2 - 5). PZT drive. FSD interface.

1.16 Operability/Maintenance: Each LLRF system shall have the ability of being taken off line and removed with no impact to the HPA or beam operations.

1.17 Compatibility with present cryomodules and HPA: The new LLRF system shall be backward compatible with the present accelerating systems and their subsystems. In no way shall this requirement minimize, negate or override any performance requirements contained in this document, such that the EU upgrade cryomodules performance is derated.

1.18 Operational Lifetime: The LLRF system shall have useful lifetime of 25 years.

1.19 Process Variables

A set of Common Process Variables shall be used by EPICS to control and monitor the LLRF control system. Operator screens shall use only these Common Process Variables and shall not distinguish between differences in the underlying hardware. A set of hardware-specific Special Process Variables shall be used for Expert screens. The process variables shall be similar or if not the same as existing LLRF variables.

1.20 RF System General Requirements

Table 1.20 RF System General Requirements

Frequency:	1497 MHz
Bandwidth (3 dB)	1 MHz
Intermediate Frequency (IF)	70 MHz @ 0 dBm, front panel, SMA
Local Oscillator Frequency (LO)	1427 MHz @ 20 dBm, front panel, SMA
Cavity Q_L	$2x10^7$
RF Power	13 kW (1 dB compression, 14 kW saturated)
Cavity Micro phonic detuning (max)	2 Hz stdev. and 20 Hz peak.
Lorentz detuning coefficient (max)	2 Hz/ $[MV/m]^2$

LLRF Control System Functional Requirements

2.0 LLRF CONTROL SYSTEM

The LLRF Control Module shall be the core of the LLRF system and shall be responsible for all aspects of cavity monitor and control including resonance control, maintaining cavity voltage, fault processing, etc. The functional requirements describe in detail the features whether in software or hardware to be implemented by the new LLRF system.

2.1 Non-Feedback Functionalities

This section outlines some required features of the LLRF control system that are not directly related to the feedback processes the LLRF control system shall provide.

2.1.1 Mechanical and Piezoelectric Tuner Monitor and Control

The LLRF control system shall configure and drive the tuners.
The LLRF control system shall allow manual tuner control of the tuners through the accelerator's distributed control system.
The LLRF control system shall provide periodic updates to the accelerators distributed control system as to tuner position, limit switch status, direction, etc.

2.1.2 Fault Detection/Report/Reset/Recovery

The system shall automatically recover from an interlock-initiated trip out of RF and reestablish RF in the cavity once safe operating conditions have returned (e.g. vacuum levels have returned to normal). The requirement shall be to recover from faults within 0.1 seconds of the return of a normal operating environment. The physics related to the fault (excessive Lorentz detuning, etc.) may limit recovery time, but the system shall strive to recover RF as quickly as possible in these situations.

2.1.3 History Buffers

The LLRF system will collect and maintain waveform data for the class of signals below. The data will be collected in CW or pulsed mode. Each data set will contain 200 ms of data. The system must have the capability to trigger on a fault with 100 ms of pre and post data available. These are the signals of interest but the system must be configurable such that any signals processed by the FPGA can be made available.

Signals:
Incident RF power
Reflected RF power
Cavity Field (transmitted power)
I and Q drive signals
Internal Diagnostic Signals (loop error, etc.)
Signal statistics for these history buffers will be available on an event-by-event basis (i.e. either an RF/cavity trip or beam initiated FSD).

2.1.4 Self-diagnostic capabilities

The system shall have self-diagnostic capabilities that identify and flag hardware and control problems in the LLRF system.

2.1.5 Shutdown LLRF system

The LLRF system shall shut down the RF drive within 10 μs in response to a cavity interlock fault.

2.1.6 Pulsed mode operation

The system shall support pulsed mode operation using a signal with the following characteristics:

Repetition Rate	<1 kHz
Duty Cycle	Variable 1 – 100 %
Open Loop Duty Cycle	> 10 %
Input Impedance	10 kΩ
Connector Type:	Lemo

Lock up time (of the feedback loop) should depend on the cavity fill time and not the speed of the LLRF system

2.1.7 Operability

The system shall be hot swappable. It shall be possible to swap out the LLRF control system without disrupting the operations of neighboring LLRF control system modules and their cavity systems and with minimum impact on beam operations.

2.1.8 RF system maintenance procedures

RF system maintenance procedures that require more than the LLRF system itself to achieve optimal RF system performance are required. This implies that LLRF system shall provide support for the following: High Pulsed Power Processing (HP4) for waveguide cleaning, Direct Voltage Controlled Oscillator (VCO) operation (or DDS like operation) to support RF commissioning activities, and Helium Processing to remove surface impurities from cavity walls.

2.2 Major Feedback Functionalities

2.2.1 The LLRF control system shall be responsible for processing the raw data acquired by the LLRF data acquisition system to perform feedback control for the cavity.

2.2.2 Cavity Voltage Stabilization.

2.2.3 The system shall maintain the amplitude and phase of the electromagnetic field in the cavity to (whatever spec) by driving klystron output.

2.2.4 The system shall recognize and generate flags when it loses gradient or phase lock for a short period of time (1-5 ms).

2.2.5 It shall be possible to enable and disable cavity voltage stabilization which means it shall be possible to run the RF system in open loop or closed loop mode.

2.2.6 Lorentz Compensator

The system shall provide compensation for Lorentz force detuning using a piezoelectric or magnetostrictive tuner.

2.2.7 CW Resonance Control/Auto-track

Auto-track compensates for drifts in the cavity resonance by purposefully deforming the cavity's mechanical structure.

- The system shall use mechanical and/or piezoelectric tuners to maintain cavity resonance to 5 Hz (mechanical tuner) and 1 Hz (piezoelectric tuner).
- It shall be possible to turn off auto-track mode to allow manual tuner adjustments. When auto-track is reengaged, it shall resume resonance tracking from the present tuner positions.

2.2.8 Resonance Hunting/Auto-tune/Ptune

The LLRF system should bring a cavity in from 20 bandwidths away from resonance in less than 1 minute to within 2 Hz of resonance. At a minimum the system shall bring a cavity that is 5 kHz from 1497 MHz on resonance in less than 30 seconds. Ultimately, the system should be able to recover a cavity that is 30 kHz out in 5 minutes or less. When turning on from idle to find cavity resonance, amplitude regulation requirements are relaxed to 1 %, and there is no phase regulation requirement imposed.

2.2.9 Feed Forward Including Adaptive Feed Forward

The system shall support feed forward, but feed forward algorithms shall not be critical to cavity resonance control. It shall be possible to enable and disable the feed forward mechanism. When feed forwarded is enabled, it shall run in accordance with the operational mode (pulsed or CW) of the RF system.

2.3 Interoperability with Systems Out side the LLRF Control System

As a subsystem of an accelerator, the LLRF control system necessarily shall interact with other accelerator subsystems. This section describes how the LLRF control system shall interact with other subsystems of the accelerator.

2.3.1 High Power Amplifier (HPA) and Cathode Power Supply (CPS) Interface

The HPA/CPS system provides power to the klystron that in turn provides the power used to establish voltage in the cavity. The HPA/CPS and LLRF systems are naturally dependent on each other. This section describes the interface between these two related systems.

- The HPA and CPS controls shall be separate from the LLRF controls.
- The following permission signals for each cavity/klystron pair shall be directly communicated between the two systems:
  HPA/CPS to LLRF
  Ready for RF
  Fast RF Shut Off
  LLRF to HPS/CPS
  High Voltage Permit
  Klystron Drive
  Communication protocol to be determined during design.

- Other signals such as cavity forward and reflected power values shall be available through the accelerator's distributed control system (EPICS).

2.3.2 Fast Energy Vernier Interface (for fast Linac energy lock system)

The accelerator may have a beam-based fast feedback system that compensates for small drifts in beam energy by adjusting the cavity gradient. The LLRF system shall accept an external input signal from a fast linac energy lock system to adjust the cavity gradient. Interface is described in 4.6.0.

2.3.3 Interface to Distributed Event Trigger System

For beam physics experiments and RF system diagnosis, it is useful to trigger data collection around the machine from various systems in a synchronized fashion. To this end, the system shall accept an event trigger input to initiate special data acquisition sequences.

2.3.4 Interoperability with the Accelerator's Distributed Control System

The LLRF control system shall operate in an environment that is compatible with the accelerator distributed control system (presently, the Experimental Physics and Industrial Control System, EPICS). Compatibility with the control system is not limited to the physical hardware and network connections and operations. It, also, entails compliance with the control system software group's software life cycle procedures and tools.

2.4 Requirements for Accelerator's Distributed Control System

This section outlines the requirements for the distributed control system. The requirements for the front-end computer are outlined first, followed by the general-purpose host level data management requirements. Lastly, the RF system management requirements are presented.

2.4.1 Front-End Level Requirements

The distributed control system software running on the front-end computers shall serve a supervisory role in the system acting as a window into the LLRF control system. It shall not be integral to the cavity control process.

Signals or classes of signals that shall be written to or read directly from or derived from data from the LLRF system shall include (but may not be limited to) the following:

- Normal Operations Mode Signals
  Gradient Setpoint/Readback (MV/m) with 0.1 % resolution
  Phase Setpoint/Readback (Degrees) with 0.1-degree resolution
  Forward/Reflected Power
  Cavity/Zone RF On/Off
  RF On Time
  Amplifier On/Off
  Cavity/Zone Bypass
  Faults/Status
  Fault Occurred (y/n)
  Analog Waveform related data
  Trip analysis/sequence of events
  Ops Level Status Information (RF good/RF bad)

Ops Level Cavity Resonance Stability Status similar to what is available from the RF Commander medm screen (Tuning, SOS, etc.)
LLRF System Lost Gradient Lock (y/n)
LLRF System Lost Phase Lock (y/n)
Zone Gang Phase Offset
Linac Gang Phase Offset
HP4 support
Helium processing support
Temperature Diode Readbacks
Low Level RF Heartbeat
Configurable Stepper Motor Maximum Steps (default initially to 50000 steps)

- Expert Mode Signals

Control Algorithm Gains (e.g. Proportional, Integral, and Differential Gains)
Loop Gains
Integration Limits
Integration Time
Rotation Matrix Parameters
Open/Close Loop switches
Feed forward look up table data
Decimation factors
Decimation filter coefficients
Programmable delay settings
Spare ADC and DAC channels
Stepper Motor Configuration Parameters (such as ramp)
Piezoelectric Tuner Configuration Parameters
Amplitude, Phase, I, and Q error signals

2.4.1.1. The front-end computer shall provide access to history buffer data from the LLRF system on-demand within 100 ms. It shall provide on-going periodic updates for the statistics related to the history buffer data.

2.4.1.2 It shall be possible to control/drive the mechanical and piezoelectric tuners through the distributed control system.

2.4.1.3 The distributed control system shall be responsible for all data communications from the front-end computer to the outside world.

2.4.2 General Purpose Host Level Data Management Requirements

2.4.2.1 Alarms

- The ability to view and display alarms similar to what is presently available is required.
- An alarm server that interprets RF system alarm information in the context of operating mode similar to the RF alarm server presently in use is required to produce meaningful RF alarms for the upgraded RF system.

2.4.2.2 Data Archiving

- Data archive capabilities similar to what is in existence now are required to support fault analysis, component lifespan analysis, overall system performance, and system interoperability studies (e.g. interactions between RF system and energy locks).

- Waveform archiving to provide a time history of waveform data (history buffers) collected by the low level RF system is required.

2.4.2.3 Data Save and Restore

- Data associated with a machine configuration must be saved and available for restore to the front-end computer in order to reestablish the RF parameters for a particular accelerator operations configuration (e.g. 4 GeV beam operations, 6 GeV beam operations, etc.).
- A bump less or warm reboot capability is required for front-end computer reboots and LLRF system resets. This means that a subset of RF data must be periodically saved and available for automatic or on-demand restore to the RF system after a front-end computer reboot or LLRF system reset to reestablish the operational state of the system prior to the interruption.

2.4.3 RF High-Level Functionality Applications

Applications that consider the behavior of all of the cavities as a system or its interaction with other systems such as the following notable examples are required.

2.4.3.1 An application similar to Krest, which is a beam based tool that ensures the cavities are operated on crest (beam phase is the same as the cavity phase) by performing cavity-by-cavity and zone-by-zone phasing is required.

2.4.3.2 Applications similar to LEMi (Linac Energy Management for the Injector) and LEM (Linac Energy Management for the North and South Linacs) are required to set up the optics lattice and to distribute desired energy gain across a linac segment taking into account operational drive highs limitations, cryogenic heat load considerations, fast and slow energy lock cavity headroom requirements, cavity trip rate models, cavity operational state, etc. A related application similar to Fudge It that sets the linac fudge factors used in the LEM applications is also required.

2.4.3.3 RF performance analysis tools similar to the RF Fault Counter, Cavity Status/History, RF Analyzing Tool (RAT), and gradient calibration are required to maintain and improve operability of the RF system. These tools shall have access to and respond to the LLRF lost gradient and phase lock flags as necessary.

Transceiver Requirements

3.0 TRANSCEIVER

The new LLRF control module requires a transceiver capable of detecting moderate-level (+20 dBm) signals, while preserving linearity and providing high-resolution phase and amplitude measurement. The system should include temperature compensation, in-situ performance monitoring, and on-board diagnostics. In addition, embedding numerical routines relaxes requirements for subsequent higher-level EPICS processing.

The transceiver will be designed to maintain the top-level control requirements (Table 1.1 in chapter 1.1), specifically cavity field control. The following specifications reflect those and the rest of the requirements of chapter 1.0.

3.1.0 Receiver Requirements and Considerations

The receiver portion of the Control Module consists of a single channel for Cavity Field measurement, as well as 3 general-purpose receive chains for measuring forward power, reflected power, and Master Oscillator (as a baseline reference).

3.1.1 1497 MHz Power Levels

1497 MHz power level from the Cavity Field Probe shall be in the range from -10 dBm to +20 dBm. Input damage threshold should be > +25 dBm.

Forward power, reflected power, MO and utility RF inputs should not exceed + 20 dBm in strength. Input damage threshold should be > +25 dBm.

3.1.2 Signal-to-Noise

Cavity field receive channel should have an S/N ratio of >= 80 dB, which is required to preserve phase measurement resolution. This does not include ADC specification.

Forward power, reflected power, MO, and utility receivers shall have an S/N of >= 60 dB.

3.1.3 Noise Figure

Tangential sensitivity (TS) must be consistent with S/N requirement and dynamic range. Therefore, a TS of -80 dBm is required. For a receiver having BW=8 MHz, this translates to a 25 dB Noise Figure.

3.1.4 Phase Noise Limit

Total phase noise for LO and ADC clock shall remain < 3 ps (10 Hz – 100 kHz) .

3.1.5 Stability

Stability requirements shall be imposed over a 20 dB dynamic range.

Amplitude stability should remain +/- 0.05 dB over the 10C < x < 40 C range. This can be accomplished with analog and/or digital means, provided the latency requirement is fulfilled.

Phase stability variation must be within 0.5 ps / degree C over the temperature range 10 C < x < 40 C (~ 0.3 degrees per degree C at 1497 MHz). This represents an overall bound of 15 ps (+/- 4 degrees at 1497 MHz) with constant slope. This can be accomplished with analog and/or digital means, provided the latency requirement is fulfilled. Possible examples include using additional MO inputs, dead-reckoning, and look-up-table compensation.

The following requirements were determined in accordance with accepted industry practices:

3.1.6 Linearity

The strict requirement of the receiver, being in a control loop, is monotonicity. However, the large dynamic range and moderate S/N requirements prescribe a linearity no worse than 0.1%, full scale. At maximum input (+20 dBm), a 60 dBc inter-modulation distortion (IMD) is maintained for receiver having a third-order input intercept point (IIP3) of +40 dBm.

3.1.7 Dynamic Range

Cavity field control shall meet the stated requirements over a dynamic range of 20 dB (10: 1 in gradient). Additional control is available for smaller gradients, but at reduced performance levels.

3.1.8 Receiver Bandwidth

RF bandwidth shall be > 5 MHz so as to preserve 100 ns latency.

3.1.9 Latency / Group Delay

A 1us latency requirement puts hard limitations on both numerical capacity and analog filter specifications. A group delay of <100 ns is preferred for the entire RF front end, most of which is incurred by the 70 MHz IF filter. Therefore, bandwidths narrower than 8 MHz should be avoided. Overshoot should be maintained below 10%.

3.1.10 Receiver Input Impedance

Receiver Input impedances shall be 50 Ohms, with a maximum VSWR of 1.1: 1
(or, total Return Loss > 26 dB).

3.1.11 Isolation and Carrier to Interference ratio (C/I)

In-band interference (0 – 10 Mhz), either from IMD or from neighboring channels, shall be kept below 60 dBc over the 20 dB active control range to minimize total harmonic distortion (THD).

3.1.12 1427 MHz Local Oscillator Input

Signal Level to the receiver will be +20 dBm (100 mW).

Input Impedance of the LO Port shall be 50 Ohms, with VSWR < 1.5:1 (or total Return Loss > 14 dB).

3.2 Transmitter

The transmitter portion of the Control Module consists of 2 up converter chains, one of which is for cavity control, and the other for use as a general-purpose signal source.

3.2.1 Power Levels

The output power from either channel shall be at least +0 dBm when the output DAC is driven to full-scale. This ensures proper drive for the intermediate power amplifier (IPA) and high power amplifier (HPA) systems.

3.2.2 Dynamic Range

The output power shall be able to cover 30 dB utilizing 14 bits in order to guarantee proper resolution for gradient control.

3.2.3 Output Signal Quality

Signals produced by the transmitter are amplified by a solid-state preamplifier, followed by a klystron. Spectral limitations are imposed so as to not excessively modulate the klystron, resulting in saturation and reduced availability/controllability.

3.2.4 Harmonic Content

Harmonically-related products should be below -30 dBc.

3.2.5 Spurious/LO Bleed-through

In-band (0-10 MHz) spurious should be -70 dBc. Near-frequency (LO leakage) should be below -20 dBc at the low end of the transmitters dynamic range to limit saturation and 3^{rd}-order effects on the subsequent IPA/HPA chain.

3.2.6 Output Impedance

Output impedances shall be 50 Ohms, with a maximum VSWR of 1.5: 1
(or, total Return Loss > 14 dB).

3.3 Analog-to-Digital Converter (ADC) Requirements

On-board sampling clock is available at 56 MHz, and was designed to facilitate I/Q sampling of a 70 MHz IF, using a high-speed, 14-bit ADC. If this is not the case, of if a different IF frequency is used, additional clocks must be provided.

3.3.1 Resolution

> = 14 bits

3.3.2 Output Sample Rate

> 10 MSps in order to fulfill Nyquist criteria for 1 MHz output BW.

3.3.3 Latency

< 60 ns

3.3.4 Timing Jitter (aperture)

< 500 fs

3.3.5 Linearity
Differential +/- 1.5 LSB
Integral +/- 1 LSB

3.3.6 Relative Accuracy
+/- 1.5 LSB

3.3.7 SNR
> 70 dBc (0.1 Hz to 1 MHz)

3.3.8 Spurious-Free Dynamic Range
> 80 dBc (0.1 Hz to 1 MHz)

3.3.9 THD
< -80 dB

3.4 General Considerations

3.4.1 Temperature Monitoring
The Transceiver Section shall be able to monitor and report thermal variations on order of 0.2 degrees C, for the purpose of performance compensation. Absolute accuracy, although less important, should be within 1 degree C.

3.4.2 Power Supply
On-board regulation shall be provided, so as to limit "nominal" system power supply variations from affecting Transceiver performance. Maximum power dissipation shall be kept below 10 W.
60 Hz and the higher harmonics shall be no larger than 0.001% at the output of the regulator.

3.4.3 Connectors
All RF connectors shall be of type subminiature version A (SMA), and available on the front panel.

3.4.4 Obsolescence
To the extent possible, components shall be selected with future availability and maintainability in mind. 5-year serviceability is nominal. Proprietary or specialized components shall be identified or provided for sparing.

3.4.5 Maintenance
Transceiver design should facilitate troubleshooting and diagnostics by providing clean design practices and test probe points. Transceiver must support loop back testing. Along with the 1497 MHz receive and 1427 MHz LO signals, each zone has available 10 MHz (+7 dBm) and 70 MHz (+0 dBm) which are Master Oscillator derived. They are intended to be used as general utility references, but are available for additional instrumentation or diagnostics.

Table 3.1: Transceiver Requirements Summary

Parameter	*Value*	*Imposed Qty.*		
Receiver				
C/I	60 dB	0.1 degree Phase Resolution Gradient accuracy		
S/N	80 dB	0.01% Gradient resolution		
Bandwidth	8 MHz	Latency, S/N		
Latency	100 ns	Control BW		
Noise Figure	25 dB	S/N for phase resolution		
Linearity	0.01% F.S.	Controllability		
Dynamic Range	+40 dBm IP3	Gradient accuracy		
Channel Isolation	60 dB	Phase resolution/accuracy		
Overall Jitter (clock, LO, etc.)	3 ps	Phase resolution		
Input Power Levels	RF: -10 < x < +20 dBm LO: +20 dBm			
RF Input Impedance / VSWR	50 Ohm / 1.1:1			
LO Input Impedance / VSWR	50 Ohm / 1.5:1			
In-band IMD	60 dBc	THD		
Out-of-Band IMD	30 dBc	Linearity		
Long-term Stability	0.5 ps / degree C 15 ps max. 10C < T < 40C	Long-term energy stability		
ADC		Typical 14-bit converter....		
Resolution	14 bits			
Output Sample Rate	> 10 Msps			
Latency	< 10 ns			
Linearity	Differential: +/- 1.5 LSB Integral: +/- 1 LSB			
Jitter	< 500 fs			
Transmitter				
Output Impedance / VSWR	50 Ohm / 1.5:1			
Dynamic Range	> 30 dB			
DAC Resolution	14 bits			
Output Power Level	0 dBm Full Scale (DAC)	Full klystron drive level		
Connectors	SMA			
Power Consumption	< 10 W	Motherboard & Crate P/S		
Temperature Range	10 C < T < +40 C	Service Bldg. Temperatures		

Digital System Requirements

4.0 DIGITAL SYSTEM BOARD

4.1 The digital sub-system of the Low Level Radio Frequency (LLRF) Control system, based on FPGA technology, shall contain necessary hardware to support the implementation of the requirements as outlined in all sections of this document.

4.2 The chosen FPGA shall have enough processing power to handle Non-Feedback Functions as well as Major Feedback Functionalities. The FPGA shall support a soft-core processor such that it can be an EPICS input output computer.

4.3 A minimum of 200 Kbytes/channel of memory for each History Buffers.

4.4 The digital system shall be able to connect directly to the Ethernet. An on board processor shall handle the Ethernet and EPICS communication protocols as well as perform the Requirements for Accelerator's Distributed Control System. VME IOC currently performs these tasks. It shall have the following specification.

- A processor that can handle Ethernet communication protocol.
- An operating system such as Linux that can be run on such processor
- EPICS can be run with such operating system.
- Necessary resources such as RAM, ROM, Internet signaling, etc to support such processor.

4.5 A minimum of 16 Mbytes of RAM, expandable to 128 Mbytes and 16 Mbytes of ROM or NVRAM to support the processor in 4.3.

4.6 The following are inputs and output with systems outside the LLRF control system:

- HPA/CPS → LLRF
- Ready for RF : TTL input
- Fast RF Shut Off : TTL input
- LLRF → HPA/CPS
- High Voltage Permit : TTL output
- Klystron Drive : Analog output
- Beam Sync → LLRF
- Fast Feedback: Analog input ~ 1 MHz
- 60 Hz Sync : TTL input
- Safety ←→ LLRF
- FSD in : Fiber input
- FSD out : Fiber output
- Standard Ethernet modular connectors.
- Cavity Resonance Control and Interlocks
- Support standard Ethernet communication and subsystem protocol.

4.7 The following signals shall be made available at the front panel.

- Six programmable analog voltage output, 16 bit, 100 kHz, ranges from –10 to +10V.
- Two General purpose ADC's, 16 bit, 1 MHz from -10 to +10 V
- Heart Beat LED
- LED monitoring of board voltages.
- LCD monitoring of operating state and error codes
- Reset pushbutton
- Two general purpose LED

4.8 RF Transceiver Support

Provide both mechanical and electrical support to the RF Transceiver Board. The RF transceiver board is to be mounted to the Digital board.

- Mechanical Specification
- The receiver and transmitter can either be on one board or two separate boards.
- Transceiver boards are rigidly mounted on the digital board in a mother – daughter fashion.
- Electrical Specification
- Sufficient digital input to support four 16-bits ADC for the receiver.
- Sufficient digital output to support four 16-bits DAC for the transmitter.
- ± 12 Volt supplies capable of 2 Amps.
- +5 Volt supplies capable of 2 Amps.
- +3 Volt supplies capable of 2 Amps.
- Clock signals are phase locked to the 10 MHz Master Oscillator. The specification is per section 3.2.4
  A Phase Lock Loop (PLL) Specification
  3 Pico-second RMS jitter (see chapter 3.2.4).
- Four buffered TTL/LVDS compatible signals for the receiver and four for transmitter.
- Phase drift of less than 50 Pico-second over the temperature range

4.9 Operability and Maintainability

The board shall support the systems ability to be hot swappable. The motherboard and daughter board can be replaced without disrupting other modules that occupied the same housing. The board shall support self-diagnostic algorithms and loop back bench calibration routines.

5.0 Cavity Resonance Control, Heaters, and Interlocks Requirements

Cavity resonance control is achieved by adjusting the length of the cavity using a mechanical tuner. The tuner has two mechanical driving devices: a stepper motor and a Piezo tuner. Both of these devices are driven by the resonance controls. The interlocks protect from three fundamental faults, waveguide window events, cavity vacuum events and liquid helium events. Liquid helium events are slow in nature and the interlocks are derived from signals within the EPICS control system. There is a beam line vacuum system which processes the beam line vacuum signal and warm waveguide vacuum signals and provides the appropriate process variables to EPICS and hardware interlocks to the LLRF interlock interface, as well as controlling the beam line vacuum valves. The sensors for the waveguide interlocks are a photomultiplier tube for detecting arc discharges on the vacuum side, and a thermopile infrared sensor which detects waveguide and window high temperature conditions. These signals will be processed locally by the LLRF interlock interface.

There are eight resistive heaters in each cryomodule. They are used to compensate for the heat produced by the cavities during normal operations. Thus power is applied to the heaters from and SRF supplied algorithm (as it is done presently).

5.1 Resonance Control

5.1.l Stepper motor control, 4-wire DC stepper motor.

5.1.1.1 200 full steps per revolution. The electronics shall be controlling it with a micro stepper with 200 micro steps per full step or 40,000 steps per revolution.

5.1.1.2 Speed. Normal operation varies from 1 full step per second to 200 full steps per second for high speed operation. Provisions should be made for 16 bit variable speed control adjustments. This adjustment should be programmable via EPICS through the LLRF control module.

5.1.1.3 Voltage and Current ratings. The motor used in standard CEBAF cryomodules is a 20 V 200 mA, the motor used in cryomodules FEL-03 and SL21 are 24V, 220 mA motors. The controls should be adaptable via jumpers for the different motor types.

5.1.1.4 Short circuit and open circuit protection. The motor drive circuitry shall be protected from damage due to (a) a short circuit to ground, (b) winding to winding short circuit, (c) connection to the motor while energized, (d) disconnection to the motor while energized. (a) and (b) may be done using fuses or other re-setable devices. If fuses, etc. are used they will be replaceable without unplugging the module and they shall have fault indicators visible from the front of the module. (c) and (d) shall be done in such a matter that no operator interaction is required.

5.1.1.5 Limit Switches. In addition to mechanical stops, each tuner has two normally closed limit switches. The motor shall not be driven in the direction of the limit switch when the limit switch is in an open state.

5.1.1.6 Hot Swap. The drive electronics for an individual cavity shall be hot swappable while the remainder of the zone is operational. Devices common to all cavities do not have to meet this requirement.

5.1.1.7 Interface to LLRF controls. Initial design calls for a 4-wire, 2-way, serial interface for this function.

5.1.1.8 Open winding condition. It is required that the hardware detects an open winding and indicates such to EPICS.

5.1.1.9 Front panel controls and indicators. The front panel shall have an indicator that displays the state of the limit switches. It is also desirable to have a way to operate the motor from the front panel using a simple interface unit, for instance the ability to apply TTL-level pulse and direction bits to a front panel connector.

5.1.2 Piezo Tuner Controls

5.1.2.1 Voltage 0 to 500 VDC (Upper voltage TBD) SL21 and FEL3 use 150 V Piezos and will probably require modified modules.

5.1.2.2 Frequency Response: 1 kHz full bandwidth. The output will be filtered as deemed necessary by micro phonic and transfer function measurements on the production design cryomodule.

5.1.2.3 Current capabilities determined by PZT, the operating temperature of the device and the frequency response requirements.

5.1.2.4 Communication – serial DAC output from LLRF. It may be desirable to add provisions for error checking or multiple transmissions as part of algorithm.

5.1.2.5 The output connector used for the PZT will be suitable for safe operation. It shall be configured so that it can be connected and disconnected when energized.

5.1.2.6 The system shall have short circuit protection. There will be a front panel indication of a short circuit condition and an over current condition. If fuses or a hardware reset is required it shall be accessible from the front panel.

5.1.2.7 It may be desirable to have a scheme that allows an operator can control the actuator via the front panel. One possible scheme is to use an auxiliary connector and provide a 0 V to 10 V analog control voltage. This will have to be decided during the design review process.

5.1.2.8 Any stored energy devices including the actuator will be designed such that they are discharged to a safe energy level within 30 seconds.

5.2 Vacuum interlocks.

5.2.1 The standard upgrade cryomodule has no window vacuum space. Thus they will only make use of the beam line vacuum fault. This signal is produced in the vacuum interlock crate. It will be optically coupled at the input to the module. This signal will be distributed on the backplane.

5.2.2 The 5-cell cryomodule design has 4 waveguide vacuum signals in addition to the beam line vacuum. Thus there are four fault signals that need to be distributed to the cavity pairs. These signals will be optically coupled at the input to each module. The raw signals will be distributed on the backplane.

5.3 **Window interlocks**

5.3.1 Arc Detector interlock.

5.3.1.1 DC power requirement. The standard sensor is a 931B photomultiplier tube with a HC122-01 socket. The socket requires 6 to 10 V DC voltages which are converted to provide the PMT supply. The current requirement is unknown data sheet request in the works. Also the long term availability is being investigated.

5.3.1.2 Test LED. A test LED is located in the arc detector head. A 5 V pulse with a 100 ohm series resistor is applied to the LED to produce a test light pulse.

5.3.1.3 PMT signal. The PMT signal is to be terminated with a 100 Ohm resistor. The front end amplifier is a 1 MHz BW instrumentation configuration with a gain of 10. It is followed by a comparator which is set to 0.85 V. A pulse width discrimination circuit produces a latched fault signal if the optical signal has been present for more than 500 uS. Although it might be desirable to shorten this time, it can not be shorter than the tune beam pulse (250 us with a 4.3 us multipass pulse which occurs 100 us later.) as radiation from beam scraping will cause a cavity fault.

5.3.2 Window Temperature interlock.

5.3.2.1 The window temperature sensor is a thermopile which produces a signal proportional to the difference between the case temperature and the temperature of the body that it is observing. Thus for the upgrade cryomodule window heating takes the sensor from a zero voltage output to a higher voltage while, for standard CEBAF cryomodule, the signal goes from a negative voltage towards zero.

5.3.2.2 The interlock functions will occur in the firmware/software in the LLRF module. The software will scale the input signal level depending on the type of sensor and the cryomodule type.

5.3.2.3 The front end electronics and analog to digital converter shall accept both positive and negative input voltages.

5.3.2.4 Either user configurable jumpers or software controls will be implemented to change the gain of the system as necessary to accommodate both CEBAF style cryomodules (G=400) or upgrade cryomodules (G=2000, TBD).

5.3.2.5 The front end amplifier shall be an instrumentation style circuit with a bandwidth of 1 Hz. The second stage shall be a second order filter with a bandwidth of 0.3 Hz.

5.4 Heater Controls

5.4.1 Upgrade cryomodules require 8 independently controlled heaters up to 40 W each. Standard CEBAF cryomodules require 4 heaters (two in parallel) which may be independently controlled up to 80 W each at the load. The nominal heater resistance is 14 Ohms per cavity. Control will be through EPICS. It is recommended that to the merits of the device being configured as a network appliance shall be discussed early on in the design process.

5.4.2 The heaters shall be short circuit protected, line to line or line to ground, either by use of a fuse or electronic circuit. All heater supplies should function independent of the state (i.e. open or short circuit) of the other heaters. Fault status indicators shall be provided as well as feedback to the control system on the state of the heaters.

5.4.3 One side of the heater supplies shall be tied to chassis ground, or if a low side shunt is used, to a potential close to ground. If such a shunt is used it will be specifically discussed in the design review.

5.4.4 The heater controls shall be 12 bit voltage control with 12 bit read backs for individual heater voltages and currents. The accuracy of the read backs shall be better than 5% individually with a random distribution about zero.

5.4.5 It is desirable to have a 4-wire read back system for the voltage signal read at the interface to the cryomodule or at the heater interface depending on the cryomodule wiring.

5.4.6 If PWM is used for regulating the heater voltages, it shall be filtered locally or of a frequency such that there are no micro phonic interactions between the bath heating and the cavities.

5.4.7 Although heater power levels are determined by the gradient and the state of the LLRF, the hardware shall be independent of the LLRF hardware, i.e. e. a separate chassis.

5.4.8 A local read back for individual heater voltage and currents shall be provided. Such a read back shall function as a front panel indicator and shall be accurate to 5% or better.

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Chapter 4

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APPENDIX

A. Transceiver Input-Output

Front Panel

Signal Name	Input/Output	Reference Designator	Frequency	Nominal Range	Maximum (no damage)	Impedance
Cavity Transmitted	Input	RF_In_A	1497 MHz	0 to +20 dBm	+25 dBm	50 Ohm <1.1:1 VSWR
Forward Power	Input	RF_In_B	1497 MHz	-20 to +0 dBm	+13 dBm	50 Ohm < 1.5:1 VSWR
Reflected Power	Input	RF_In_C	1497 MHz	-20 to +0 dBm	+13 dBm	50 Ohm < 1.5:1 VSWR
Master Oscillator*	Input	RF_In_D	70 MHz	-10 to +0 dBm	+13 dBm	50 Ohm < 1.5:1 VSWR
Cavity Drive	Output	RF_Out_A	1497 MHz	-20 to +0 dBm	N/A	50 Ohm < 1.5:1 VSWR
Utility#	Output	RF_Out_B	1497 MHz	-20 to +0 dBm	N/A	50 Ohm < 1.5:1 VSWR

* Intended for long-term stability monitoring. Provisions are available for using either 499 MHz or 70 MHz input. Lower input dynamic range reflects necessary MO input requirements.

#Utility output default is for 1497 MHz output, but can be modified to produce 70 MHz or baseband video.

Board I/O

Signal Name	Nomenclature	I/O	Level
ADC1	**AD6645ASQ**		
Data Lines	A_IN0-A_IN13	O	3VTTL
Data Voltage Midpoint	A_DMID	O	3VTTL
Data Overrange	A_OVR	O	3VTTL
Data Ready	A_DRY	O	3VTTL
IO_Clock	ENCOD, /ENCOD	I	3VTTL/Diff'l
ADC2	**AD9245BCP**		
Data Lines	B_IN0-B_IN13	O	3VTTL

I/O Clock	CLK	I	3VTTL
Data Out-of-Range	B_OTR	O	3VTTL
ADC3	**AD9245BCP**		
Data Lines	B_IN0-B_IN13	O	3VTTL
I/O Clock	CLK	I	3VTTL
Data Out-of-Range	B_OTR	O	3VTTL
ADC4	**AD9245BCP**		
Data Lines	B_IN0-B_IN13	O	3VTTL
I/O Clock	CLK	I	3VTTL
Data Out-of-Range	B_OTR	O	3VTTL
DAC1	**AD9767AST**		
Data Lines	1D0-1D13	I	3VTTL
Input Write Signal	WRT1	I	3VTTL
I/O Clock	CLK	I	3VTTL
DAC2	**AD9767AST**		
Data Lines	1D0-1D13	I	3VTTL
Input Write Signal	WRT1	I	3VTTL
I/O Clock	CLK	I	3VTTL
DAC Power Down Control	SLEEP	I	3VTTL
Temperature Sensor	**LM92CIM**		
Serial Data Line	SDA	I/O	3VTTL
I/O Clock	SCLK	I	3VTTL
Critical Temperature Alarm	T_CRIT_A	O	Open Drain
User Set Address Inputs	TEMP_A0,A1	I	3VTTL
Interrupt Output	INT	O	Open Drain
Power Detector	**AD8361ARM**		
Low LO Power Detect	Low_Power_Det	O	3VTTL
Miscellaneous			
DAC RF Output Inhibit	TR_SWITCH	I	3VTTL
10 MHz Reference	10MHZ_REFIN1	I	TTL
Power			
+12V		Power	Analog
-12V		Power	Analog
+24V		Power	Analog
-24V		Power	Analog
RTN/GND		Power	Analog

B. Digital Section Input-Output (example)

Quantity	Description
	Front Panel
1	Ethernet 10/100 RJ-45.
1	Fiber in. Agilent HFBR-2412.
1	Fiber out. Agilent HFBR-1412.
2	TTL (0-3V) in. Lemo EPY.00.250.NTN.
6	16bits, Voltage Configurable from +10V to –10V, 500 KSamples Max DAC. Lemo EPY.00.250.NTN.
1	Analog Master Oscillator (PLL Ref) in. SMA SPC Technology 8589-0843.
2	16 bits, 100KSamples ADC, +15V to –15V ADC. Lemo EPY.00.250.NTN.
	Mate to Daughter Board. Four Samtec FW-50-05-G-D-530-135-A
142	TTL (0-3.3V) I/O
1	56 MHz TTL Clock. Driven to all four connectors.
1	5V 2Amp Digital Supply.
1	3.3V 2Amp Digital Supply
1	12V 2Amp. Analog Supply
1	-12V 2Amp. Analog Supply
	Miscellaneous
16	TTL (0-3.3V) I/O. AMP/TYCO 512-9988.
1	JTAG. AMP/TYCO A26268.